



SSC8035GS6B

P-Channel Enhancement Mode MOSFET

➤ Features

V_{DS}	V_{GS}	$R_{DS(ON)}$ Typ.	I_D
-30V	$\pm 12V$	58m Ω @-10V	-4A
		67m Ω @-4V5	
		86m Ω @-2V5	

➤ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

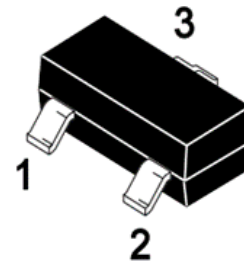
➤ Applications

- TFT panel power switch
- Portable DVD, DPF
- High side DCDC converter
- High side driver for brushless DC motor

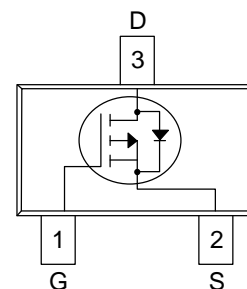
➤ Ordering Information

Device	Package	Shipping
SSC8035GS6B	SOT-23	3000/Reel

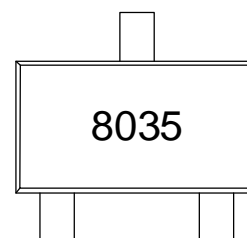
➤ Pin configuration



SOT-23



Pin Configuration (Top View)



Marking



➤ **Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-30	V
V_{GSS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current ^a	-4	A
I_{DM}	Pulsed Drain Current ^b	-16	A
P_D	Power Dissipation ^c	1.52	W
T_J	Operation junction temperature	-55~150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55~150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings ($T_A=25^{\circ}\text{C}$ unless otherwise noted)**

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a	80	104	$^{\circ}\text{C}/\text{W}$

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user is specific board design. The power dissipation is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

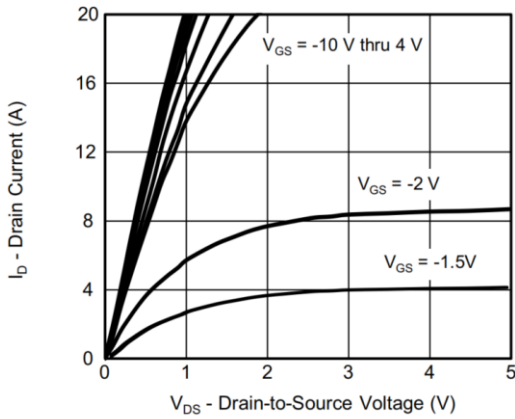


➤ **Electrical Characteristics (T_A=25°C unless otherwise noted)**

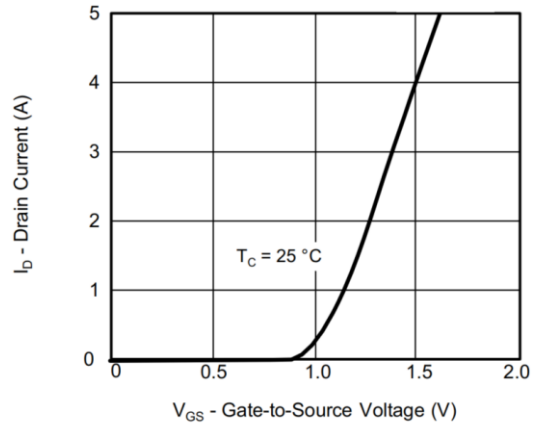
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250uA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250uA	-0.5	-0.75	-1.5	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10V, I _D = -4A		58	75	mΩ
		V _{GS} = -4.5V, I _D = -2A		67	85	
		V _{GS} = -2.5V, I _D = -1A		86	120	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -30V, V _{GS} = 0V			-1	uA
Gate-Source Leak Current	I _{GSS}	V _{GS} = ±12V, V _{DS} = 0V			±100	nA
Transconductance	G _{FS}	V _{DS} = -5V, I _D = -3A		8		s
Forward Voltage	V _{SD}	V _{GS} = 0V, I _S = -1A		-0.8	-1.3	V
Input Capacitance	C _{ISS}	V _{DS} = -15V, V _{GS} = 0V, f = 1MHz		560		pF
Output Capacitance	C _{OSS}			62		
Reverse Transfer Capacitance	C _{RSS}			52		
Turn-on Delay Time	T _{D(ON)}	V _{GS} = -10V, V _{DS} = -15V, R _L = 4Ω, R _G = 3Ω		9.5		ns
Rise Time	T _r			8		
Turn-off Delay Time	T _{D(OFF)}			31		
Fall Time	T _f			23		
Total Gate Charge	Q _G	V _{GS} = -10V, V _{DS} = -15V, I _D = -4A		11		nC
Gate to Source Charge	Q _{GS}			2.4		
Gate to Drain Charge	Q _{GD}			2.8		



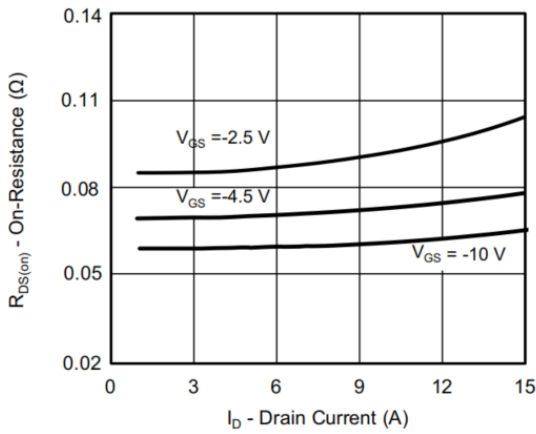
➤ **Typical Performance Characteristics (T_A=25°C unless otherwise noted)**



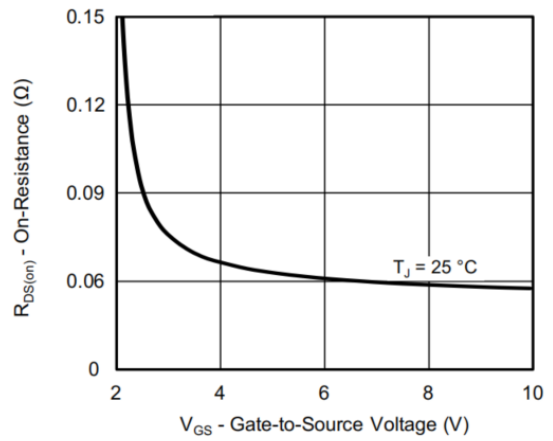
Output Characteristics



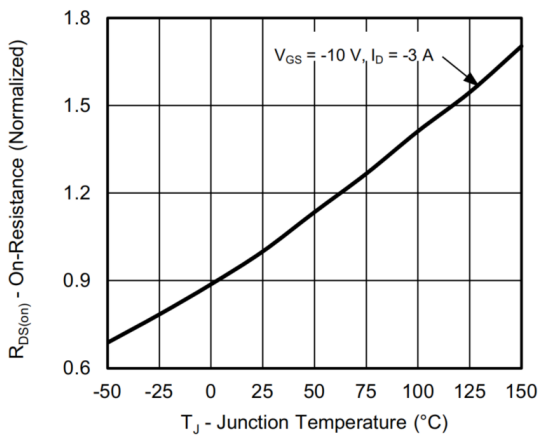
Transfer Characteristics



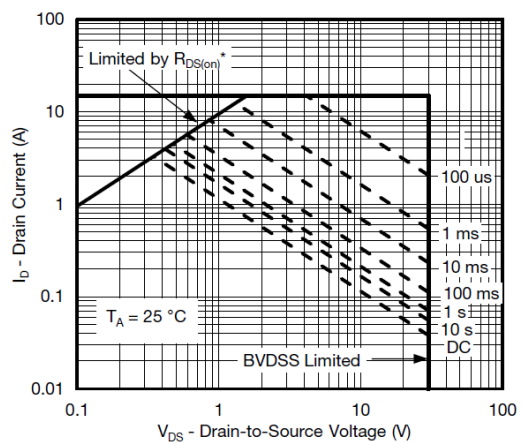
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage



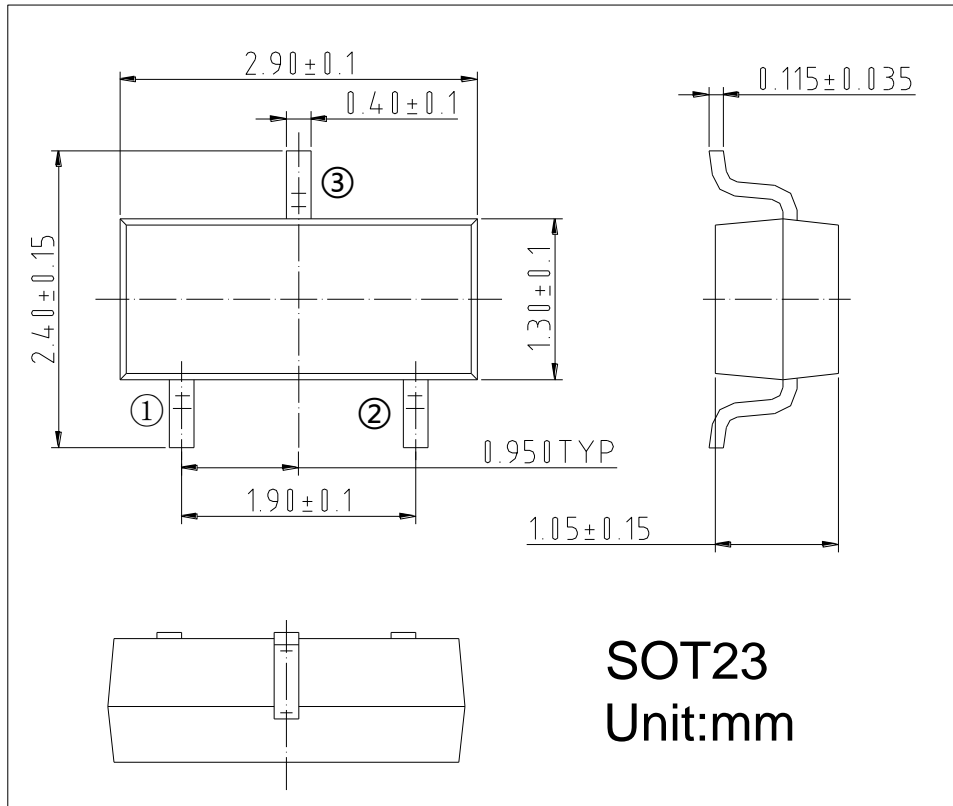
On-Resistance vs. Junction Temperature



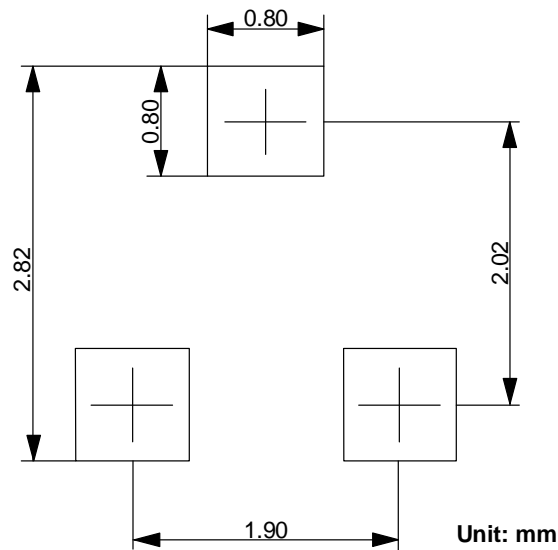
Safe Operating Area, Junction-to-Ambient



➤ Package Information



➤ Suggested Pad Layout





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